

PTO/SB/08A (10-01)
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
				Applicant / Confidential	Unknown /
				Filing Date	February 12, 2004
				First Named Inventor	Nigel G. Herron
				Art Unit	Unknown
				Examiner Name	Unknown
				Attorney Docket Number	X-1545 US
Sheet	1	of	8		

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No.¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
Di		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 6,467,009	10-15-02	Winegarden et al.	
		US- 34,363	08-31-93	Freeman	
		US- 5,072,418	12-10-91	Boutaud et al.	
		US- 5,274,570	12-28-93	Izumi et al.	
		US- 5,550,782	08-27-96	Cliff et al.	
		US- 5,347,181	09-13-94	Ashby et al.	
		US- 5,339,262	08-16-94	Rostoker et al.	
		US- 5,311,114	05-10-94	Sambamurthy et al.	
		US- 5,504,738	04-02-96	Sambamurthy et al.	
		US- 5,552,722	09-03-96	Kean	
		US- 09/991,412	11-16-01	Herron et al.	
		US- 09/991,410	11-16-01	Herron et al.	
		US- 5,457,410	10-10-95	Ting	
		US- 5,740,404	04-14-98	Baji	
		US- 5,581,745	12-03-96	Muraoka	
		US- 5,742,179	04-21-98	Sasaki	
✓		US- 5,600,845	02-04-97	Gilson	
DT		US- 5,574,930	11-12-96	Halverson Jr., et al.	

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Examiner Signature	<i>Davidson</i>	Date Considered	9/21/05
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DT		US- 5,473,267	12-05-95	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
		US- 5,737,631	04-07-98	Trimberger	
		US- 5,748,979	05-05-98	Trimberger	
		US- 09/968,446	09-28-01	Douglass et al.	
		US- 6,026,481	02-15-00	New et al.	
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		US- 5,500,943	03-19-96	Ho et al.	
		US- 2003/0062922	04-03-03	Douglass et al.	
		US- 5,809,517	09-15-98	Shimura	
		US- 5,543,640	08-06-96	Sutherland et al.	
		US- 5,574,942	11-12-96	Colwell et al.	
		US- 6,604,228	08-05-03	Patel et al.	
		US- 5,933,023	08-03-99	Young	
		US- 6,510,548	01-21-03	Squires	
		US- 6,389,558	05-14-02	Herrmann et al.	
		US- 5,732,250	03-24-98	Bates et al.	
		US- 5,889,788	03-30-99	Pressly et al.	
✓		US- 5,874,834	02-23-99	New	
DT		US- 5,835,405	11-10-98	Tsui et al.	

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Examiner Signature	<i>D. Anderson</i>	Date Considered	9/21/05
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DT		US- 6,011,407	01-04-00	New	
		US- 6,172,990	01-09-01	Deb et al.	
		US- 09/917,304	07-27-01	Douglass et al.	
		US- 5,760,607	06-02-98	Leeds et al.	
		US- 5,892,961	04-06-99	Trimberger	
		US- 6,601,227	07-29-03	Trimberger	
		US- 09/861,112	05-18-01	Dao et al.	
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		US- 6,178,541	01-23-01	Joly et al.	
		US- 6,541,991	04-01-03	Horncheck et al.	
		US- 2001/0049813	12-06-01	Chan et al.	
		US- 5,914,902	06-22-99	Lawrence et al.	
		US- 6,532,572	03-11-03	Tetelbaum	
		US- 6,154,051	11-28-00	Nguyen et al.	
		US- 6,181,163	01-30-01	Agrawal et al.	
		US- 6,356,987	03-12-02	Aulas	
		US- 6,301,696	10-09-01	Lien et al.	
		US- 6,211,697	04-03-01	Lien et al.	
✓		US- 6,163,166	12-19-00	Bielby et al.	
DT		US- 6,272,451	08-07-01	Mason et al.	

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Examiner Signature	<i>Davidson</i>	Date Considered	9/21/05
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Sheet	4	of	8		

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DT		US- 6,519,753	02-11-03	Ang	
		US- 6,434,735	08-13-02	Watkins	
		US- 6,588,006	07-01-03	Watkins	
		US- 6,539,508	03-25-03	Patrie et al.	
		US- 6,587,995	07-01-03	Duboc et al.	
		US- 6,242,945	06-05-01	New	
		US- 6,460,172	10-01-02	Insenser Farre et al.	
		US- 6,353,331	03-05-02	Shimanek	
		US- 6,507,942	01-14-03	Calderone et al.	
		US- 6,518,787	02-11-03	Allegrucci et al.	
		US- 6,611,951	08-26-03	Tetelbaum et al.	
		US- 6,522,167	02-18-03	Ansari et al.	
		US- 4,855,669	08-08-89	Mahoney	
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		US- 5,537,601	07-16-96	Kimura et al.	
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		US- 5,671,355	09-23-97	Collins	
		US- 5,752,035	05-12-98	Trimberger	
		US- 5,914,616	06-22-99	Young et al.	
DT		US- 5,970,254	10-19-99	Cooke et al.	

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Examiner Signature	Davidson	Date Considered	9/21/05
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				First Named Inventor	Nigel G. Herron
				Art Unit	Unknown
				Examiner Name	Unknown
				Attorney Docket Number	X-1545 US
Sheet	5	of	8		

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Sheet 6 of 8

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Application / C nt. N .	Unknown /
Filing Date	February 12, 2004
First Named Inventor	Nigel G. Herron
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	X-1545 US

OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issu number(s), publisher, city and/or country where published.	T ²
DT		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINL "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		MICHAEL J. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		ANDRE DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
DT		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

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DT		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		INTERNATIONAL BUSINESS MACHINES, "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
		YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC," April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
✓		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
DT		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

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DT		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch 3, pp 3-7 TO 3-17; 3-76 TO 3-87, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		INTERNATIONAL BUSINESS MACHINES, "PROCESSOR LOCAL BUS" Architecture Specifications, 32-Bit Implementation, April 2000, First Edition, V2.9, pp. 1-76, IBM Corporation, Department H83A, P.O. Box 12195, Research Triangle Park, NC 27709	
		XILINX, INC., "VIRTEX II PLATFORM FPGA HANDBOOK, December 6, 2000, v1.1, pp 33-75, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
✓		CARY D. SNYDER et al.; "Xilinx's A-to-Z System Platform"; Cahners Microprocessor; The Insider's Guide to Microprocessor Hardware; Microdesign Resources; February 26, 2001; pp. 1-5.	
DT		MIRON ABRAMOVICI et al.; Digital Systems Testing and Testable Design; Chapter 11, "Built-in Self-Test"; Computer Science Press; Copyright 1990; pp. 457-482.	

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